

Fig. 1

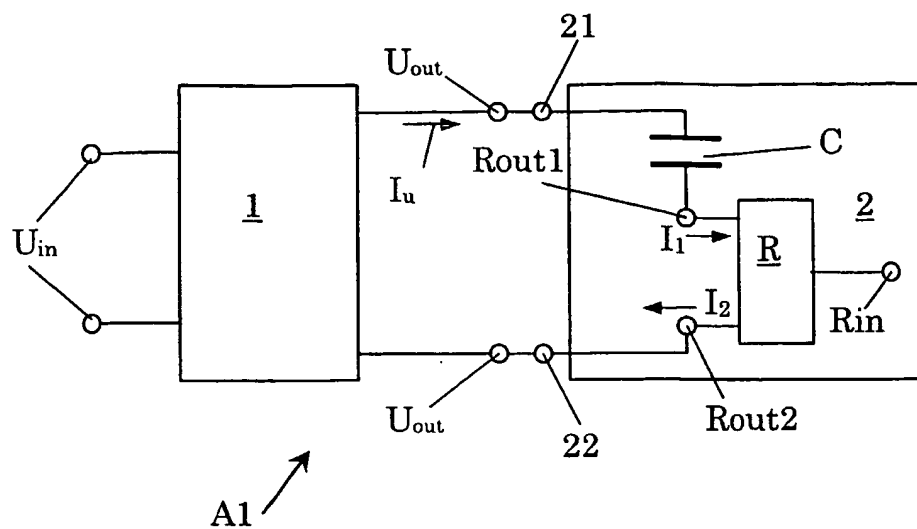


Fig. 2

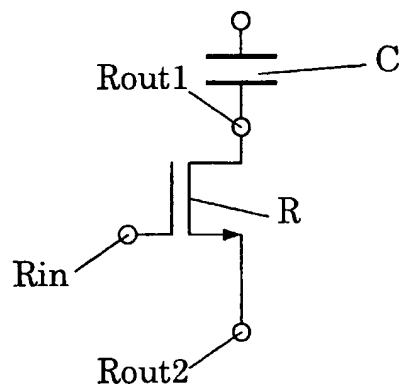


Fig. 3

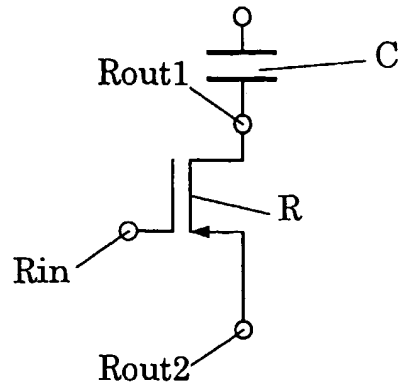


Fig. 4

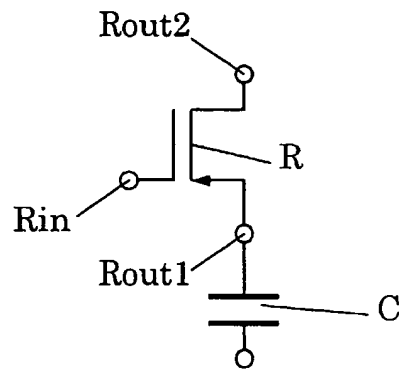


Fig. 5

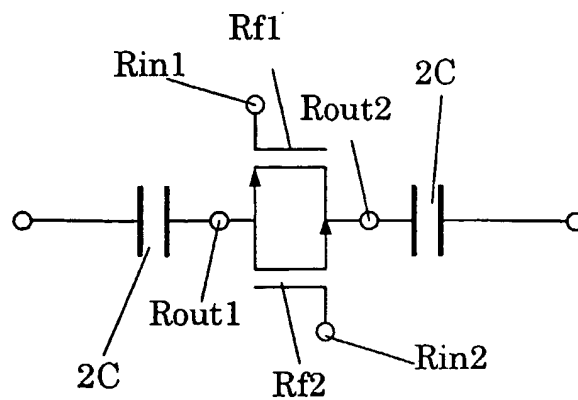


Fig. 6

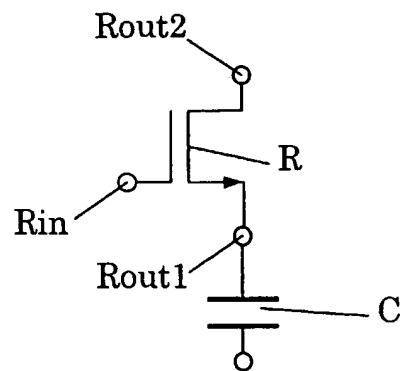
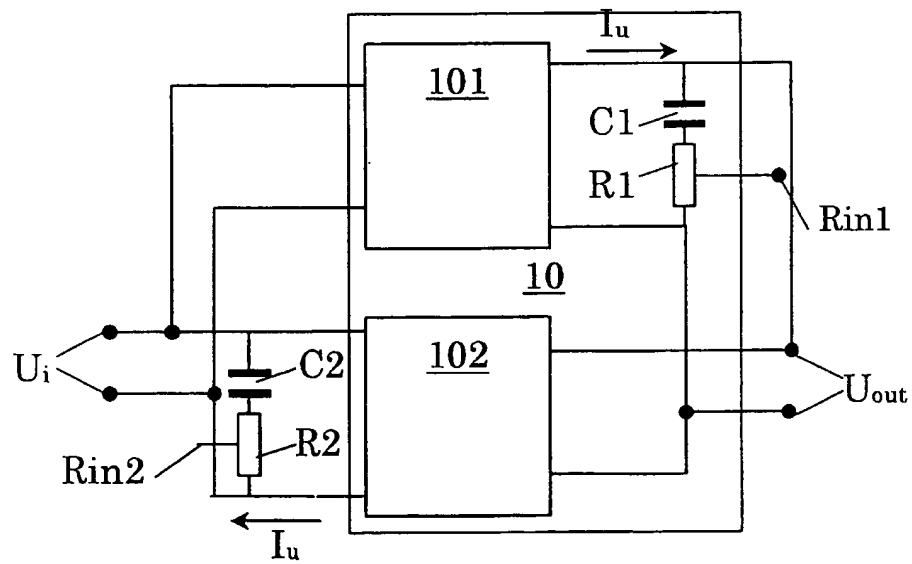


Fig. 7



The diagram shows a PLL system 200. A reference frequency f_{ref} (201) is input to a phase detector 204. The output of 204 goes through a divider 205 to a VCO 206. The VCO output (202) is fed back to the phase detector 204 and also passes through a divider 1/N 207 and a limiter 208 before returning to the phase detector 204. A dashed box encloses the VCO 206 and the divider 205. Another dashed box encloses a divider 8 and a phase-locked loop block 71. The VCO output 202 is also connected to the divider 8 and the phase-locked loop block 71. The phase-locked loop block 71 has an output 203.